System Overview

All present Psion computers are based around the proprietary SIBO architecture. A SIBO machine is a battery-powered, 8086-based, computer system. SIBO stands for SIxteen Bit Organiser. The architecture has been designed with the size, weight and power consumption of computers designed for the portable environment in mind. The key components of the SIBO architecture are:

- An 8086 class processor.
- A sophisticated power management system that selectively powers subsystems under software control.
- A synchronous, high speed, serial protocol (the Psion SIBO serial interface) for communication between a machine and its peripherals.
- Solid State Disks (SSDs) that provide fast, low-power, silicon-based mass storage with no moving parts.
- Hardware protection of the system from aberrant software processes (trapping of out of range addressing and a watch-dog timer on interrupts being disabled).
- Real-time clock.
- ROM-resident system software.
- Graphics LCD display.
- A touch sensitive digitising pad that provides a pointing device (only available on some models).
- ISDN-8bit standard combo sound system (only available on some models).

The SIBO architecture has primarily been implemented in custom ICs called ASICs. At the time of writing there are ten different SIBO ASICs. Some of these ASICs have been designed for use inside peripherals and these will discussed in detail throughout this document. All SIBO ASICs have been implemented in surface mount packages and are based on a static CMOS technology. Current SIBO products in the MC, HC and Series 3 range are based on the same three principal chips. These are the V30H (an 8086-compatible processor) and two Psion custom chips known as ASIC1 and ASIC2. Later SIBO products including the Series 3a and Workabout have these three devices integrated into a single Psion custom chip known as ASIC9. The V30H is an enhanced 16-bit CMOS version of the 8088 found in the original IBM PC. It is software compatible with the 8088. The V30H is a fully static design which means that all the internal storage elements (i.e. its registers) are made from static rather than dynamic storage components. This in turn means that there is no minimum clock speed required to refresh the storage elements and the system clock can be stopped at any time with no loss of internal state. This technique is used extensively in the SIBO architecture to save power while the processor is idle (i.e. waiting for an event).

The Psion SIBO serial protocol is a proprietary synchronous two wire serial standard by which host Psion handhelds communicate with external devices. These devices will typically be Memory Packs

(usually referred to as Solid State Disks or SSDs), RS232 and Centronics printer interfaces, fax modems, bar-code scanners, and so on. The SIBO architecture provides for two basic forms of expansion device, namely the extended internal expansion connection (as with SSDs) and the reduced external expansion connection (the 6-pin S3a serial port or the 11-pin LIF connector). The MC and HC range of computers have two SSD ports and two separate independent single row 25-way extended internal expansion ports. These ports have in addition to a Psion SIBO Channel, direct, parallel I/O from the processor. Direct connection to these machines 7.2 volt battery is included to support high power peripherals such as Printers and Barcode readers. The Series 3 range of computers have two ports for SSDs and a single, reduced, 6-pin expansion port, which provides only a Psion SIBO serial channel and limited power (<25mA). The Psion Workabout has two SSD ports, two internal expansion points, and one external expansion port. The single external expansion port uses an 11-pin Low Insertion Force (LIF) socket which provides a Psion SIBO channel, 25mA of current and additional lines required for detecting the presence of the Workabout cradle. Each internal expansion port consists of a single row 26-way connector carrying two high speed serial ports.

A range of Psion peripherals have been produced for connection to the Psion handhelds outlined above. These peripherals currently incorporate one of two custom integrated circuits (ASIC4 and ASIC5) that convert SIBO serial protocol signals to data bus TTL level voltages which enable memory and memory-mapped peripherals to be addressed. ASIC4 is used in SSDs and for memory-mapped peripherals. A typical ASIC4 peripheral for a Psion S3a would consist of an ASIC4 connected to port C of the host machine and a peripheral chip/device mapped into ASIC4's addressing space. ASIC5 is a general purpose I/O chip with a UART on board that can be run in several different modes. For example ASIC5 can be used for MCRs (magnetic card readers) or Centronics interfaces thereby simplifying peripheral design. Psion extended internal expansion ports carries an active low interrupt input line to the host controller circuitry. The reduced external expansion ports has an active high interrupt input line. The function of the interrupt can thus be programmed into the host machine's ASIC1 or ASIC9.

The low-level programming interface to a Psion handheld peripheral is encapsulated within an appropriate device driver. Psion device drivers are written in 8086 assembler and follow a prescribed pattern outlined later in this document. The construction of a peripheral and the coding of its complimentary device driver enable the developer to access its functionality through the means of library calls in a C program. Examples of such calls are `p_loadldd()` , `p_open()` and `p_close()`. I/O requests are routed through the device driver's strategy vector which maps to the PLIB `p_iow()` call. The device driver is built using the Borland Turbo Assembler and resides in a single code segment. The device driver can be stored in either RAM or a ROM on board the peripheral or can be supplied on an SSD (solid state disk).

Revision #2
Created Thu, Nov 8, 2018 9:25 AM by Alex
Updated Sun, Jun 2, 2019 8:54 AM by Alex